Intel Silicon & Manufacturing Update

Brian Krzanich
Intel Vice President
General Manager, Assembly/Test
Technology & Manufacturing Group

Sanjay Natarajan, Ph.D.
Director, 32nm Process Technology Development
Technology & Manufacturing Group

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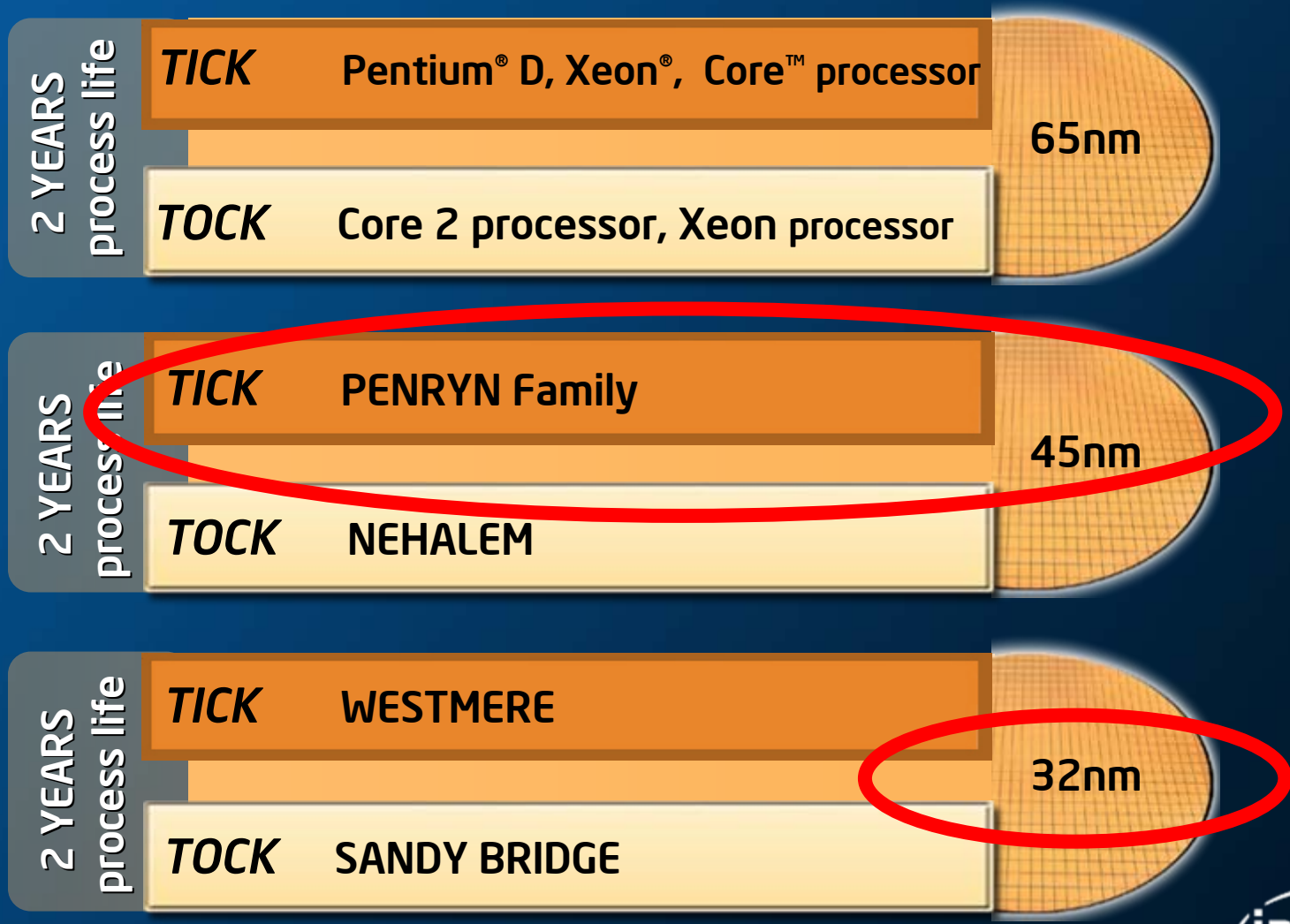
Alternating Process and Product Introductions for Sustained Leadership



45nm Status

- 1st generation revolutionary high-k + metal gate transistors for improved performance and reduced leakage power
- Working "Penryn" microprocessors were first demonstrated in January '07 and "Silverthorne" microprocessors in April '07
- Intel's 45nm processors are 100% lead-free
- Intel 45nm CPUs will convert to halogen-free packaging technology by the end of 2008
- Intel's 45 nm process technology will be described in more detail at the International Electron Devices Meeting (Dec 10-12, 2007)

High-k + Metal Gate Delivers True Performance per Watt Improvement

#1: Power Reduction
(energy efficient computing)

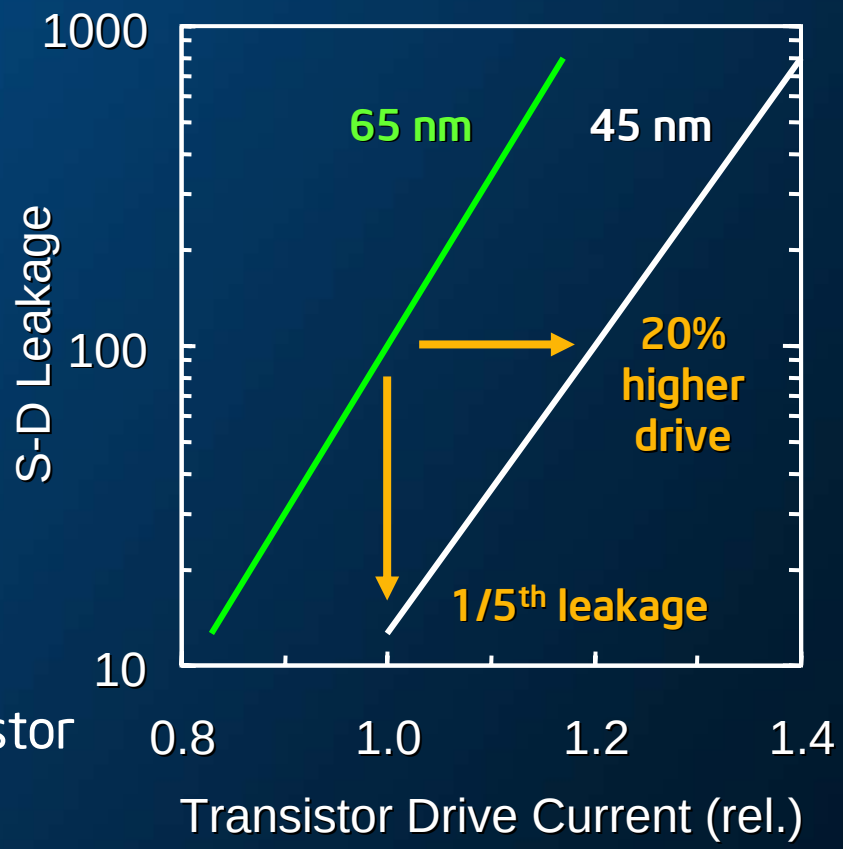
- 1/10th gate oxide leakage
- 1/5th S-D leakage

#2: Performance Increase

- 20% higher drive current

#3: Scaling

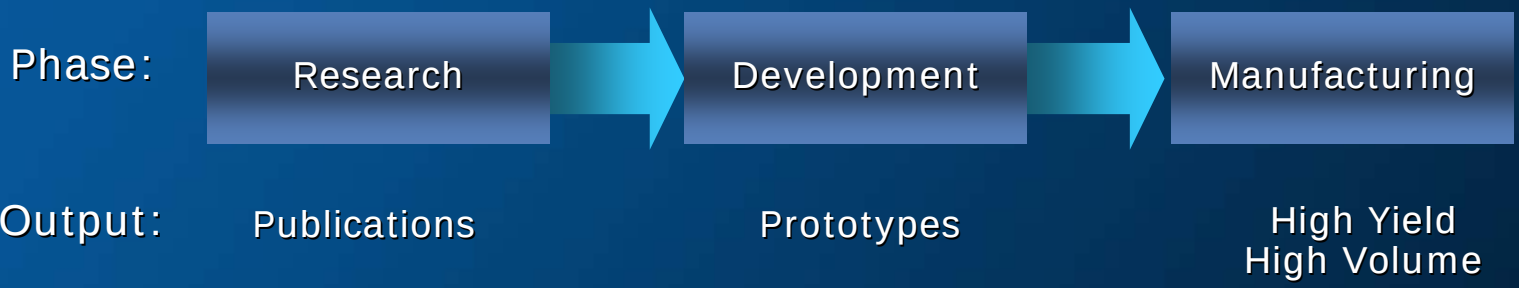
- Higher drive enables smaller transistor width for same drive strength



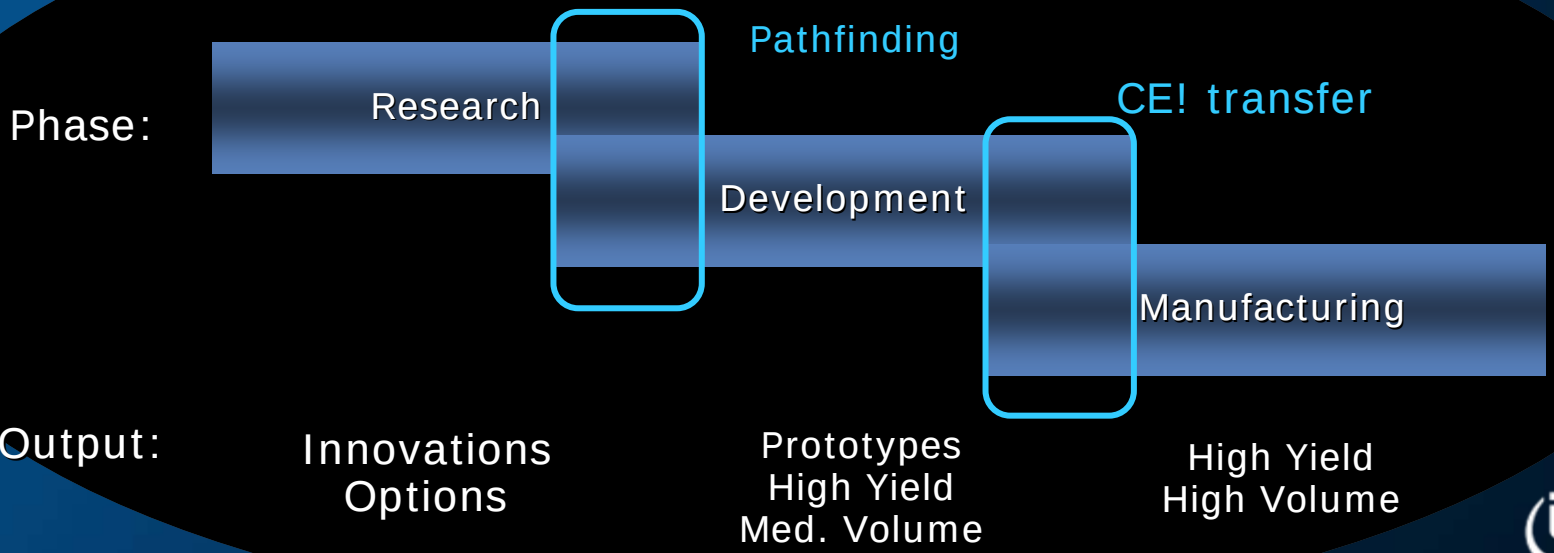
45nm Manufacturing Readiness & Operational Leadership

We Have a Well-Honed, *Unique* R-D-M Method

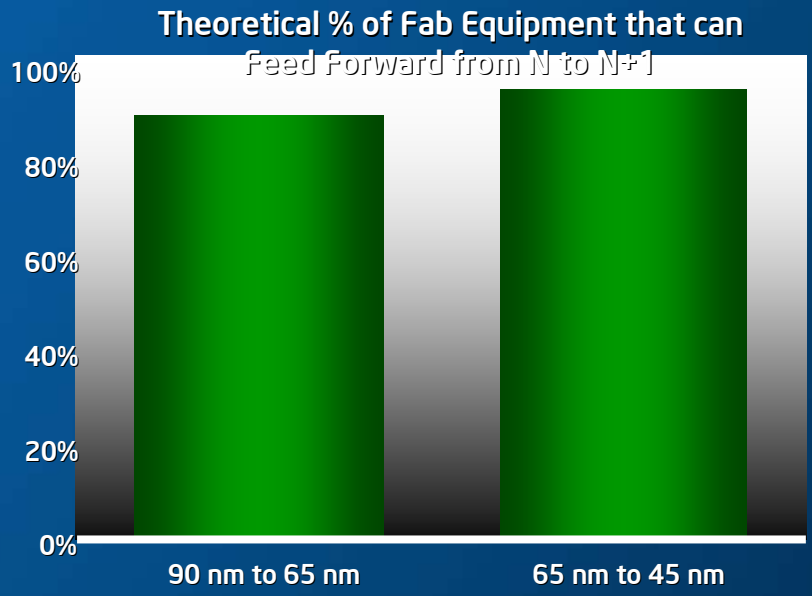
Traditional R-D-M Method:

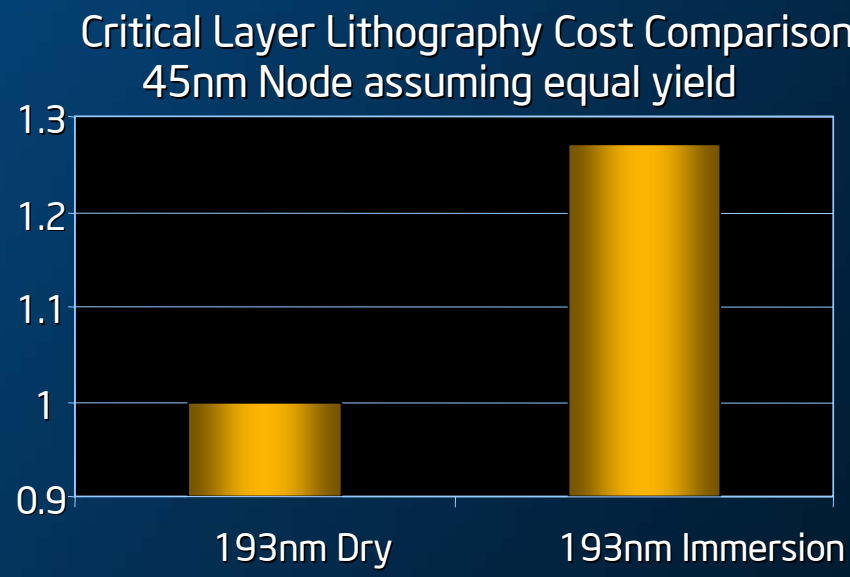


Intel's R-D-M Method:



Capital Reuse

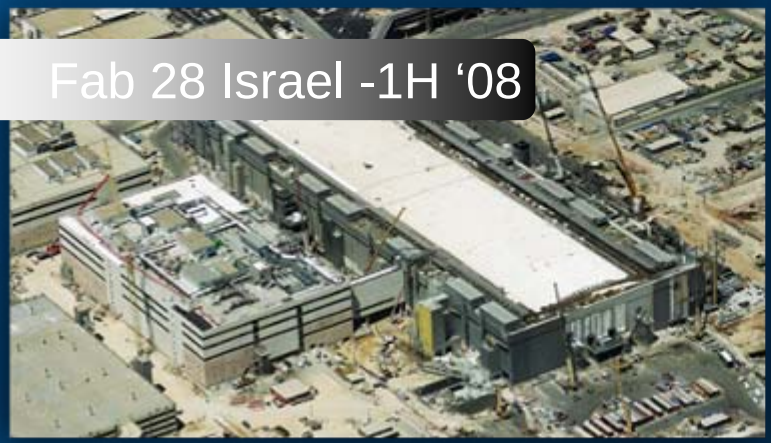




Capital Reuse Enables Predictable Ramps

Source: Intel Internal

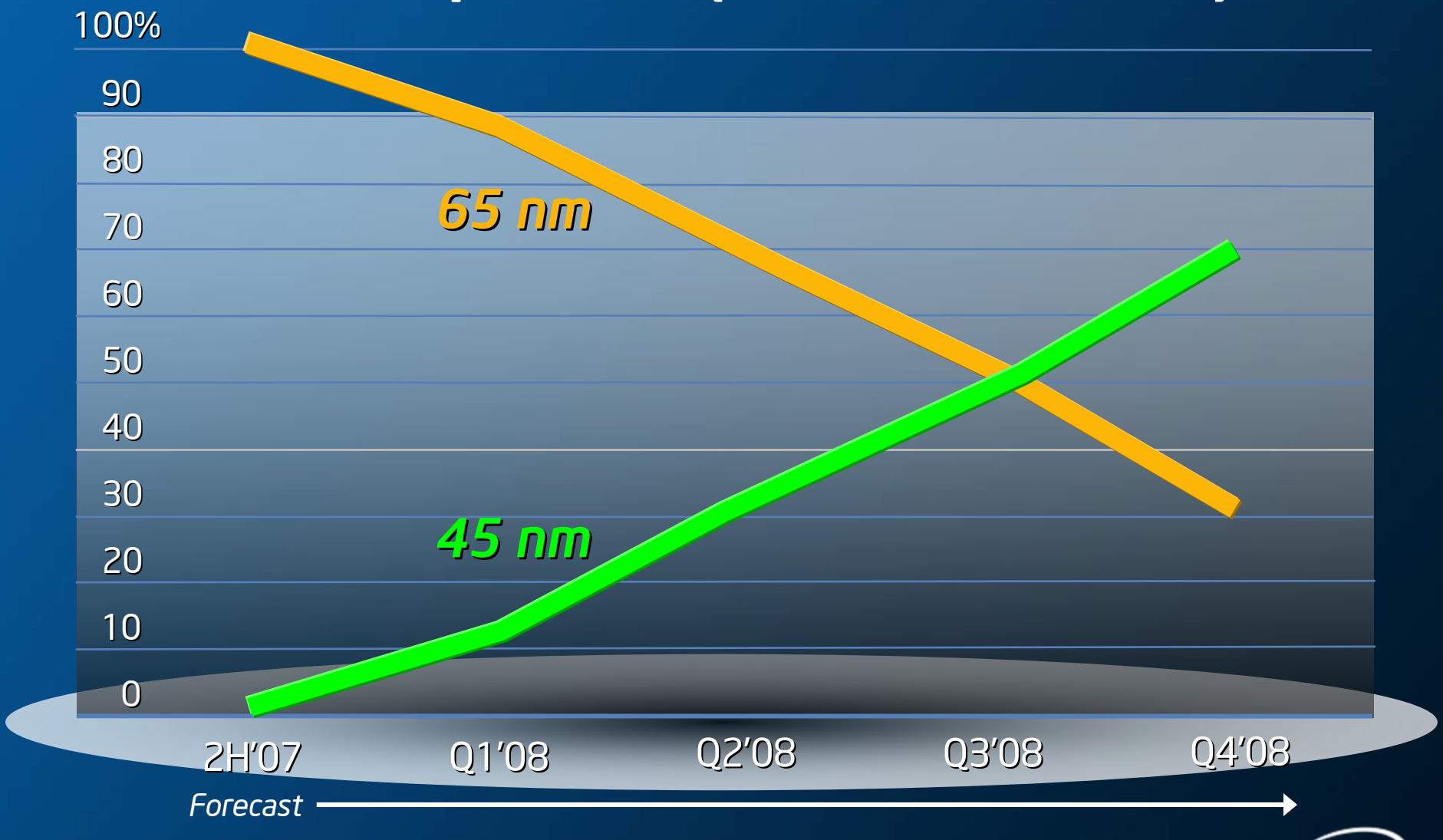
45nm Factory Network



Source: Intel

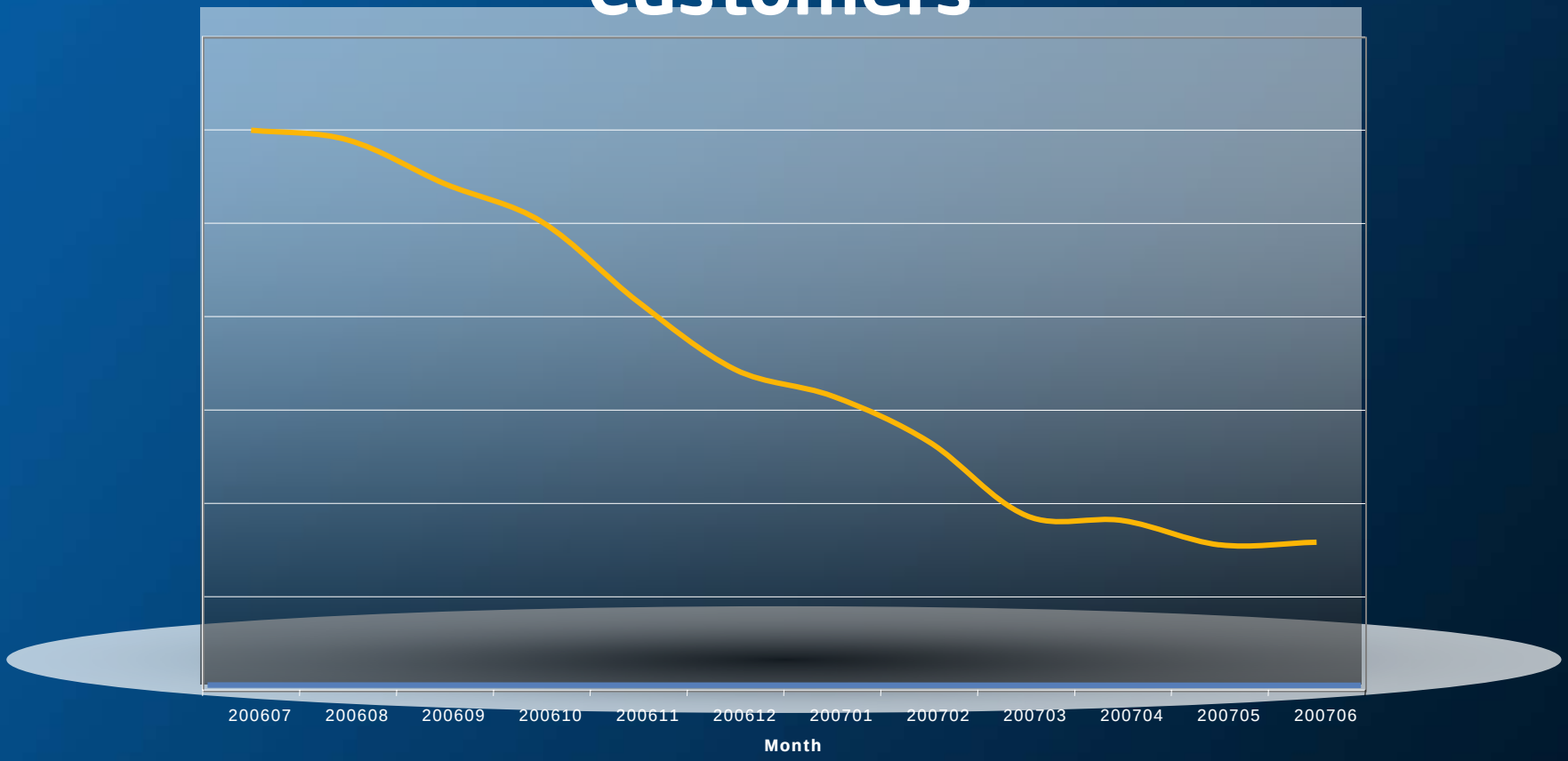
intel

CPU Shipments (65nm vs. 45nm)



Source: Intel Internal

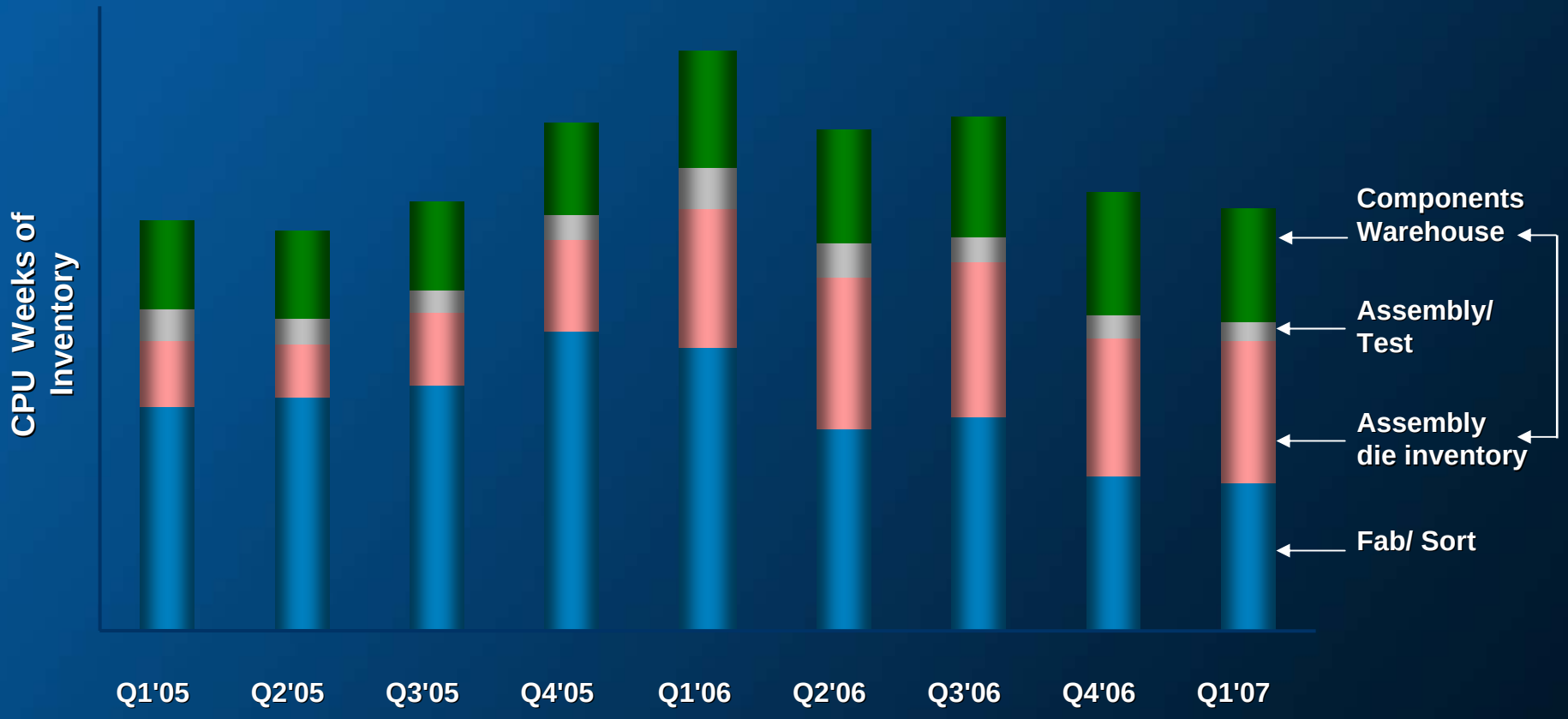
Improvements in Factory Throughput Time Increase Agility & Ability to Serve our Customers



50% Improvement in throughput time

Source: Intel Internal

Improved Manufacturing Throughput Time Drives Inventory Reductions



- **Fab and Assembly inventories cut by 50%**
- **Die and finished goods remain at desired levels**

Note: Quarterly numbers represents the last month of each quarter

Conclusions

- Sustainable Process Technology Leadership – 2 year cadence
- Well-Honed, Unique R-D-M Method
  - Copy Exactly! – cornerstone of matched yields, predictable ramps
  - 45nm Yields – on track
  - 45nm Mfg Readiness – on track
- 45nm Crossover in 2H 2008 – on track
- Continuous improvements Leading to System wide gains
  - Throughput times, Response to Customer Orders
  - Inventory Reduction
- Intel's 45nm Manufacturing - > 1 yr ahead of the competition

Most Cost Effective, Smallest, Fastest, Healthiest Products in our Customers' Hands...Earlier than Anyone Else!

Source: Intel Internal

Beyond 45nm …

Intel First to Demonstrate Working 32 nm SRAM + Logic Chips

Intel's Logic Technology Evolution

Process Name	P1264	P1266	P1268	P1270
Lithography	65 nm	45 nm	32 nm	22 nm
1st Production	2005	2007	2009	2011

Moore's Law Continues!

Intel continues to develop a new technology generation every 2 years

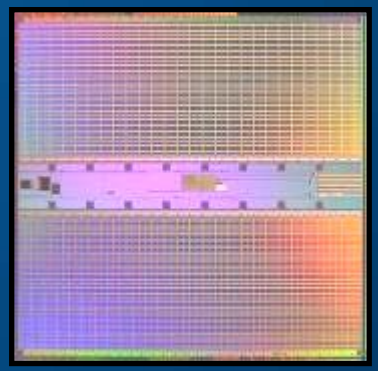
What are We Announcing Today?

- Functional 32nm 291 Mbit SRAM chips
  - Each chip with >1.9 billion transistors
- Intel first to reach this critical 32nm development milestone
- 32nm SRAM chip memory cell size of 0.182 um^2
  - ~1/2 the 45nm cell
- Uses 2nd generation high-k + metal gate transistors
- Optimized Patterning:
  - 193nm immersion lithography for critical masking layers
  - 193nm dry or 248nm dry lithography for less-critical layers
- Intel is on track to ramp 32nm logic technology in 2009

Intel SRAM Test Chips

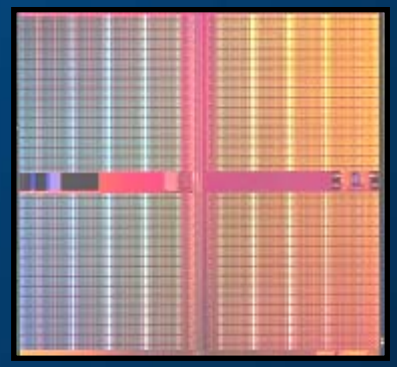
90 nm Process

1.0 um^2 cell
50 Mbit
109 mm^2
February ‘02



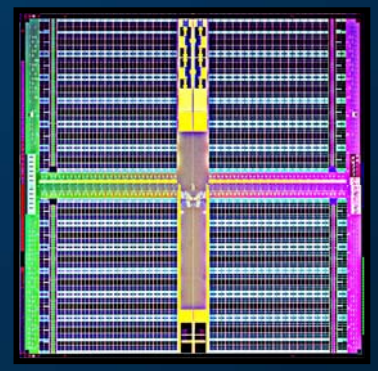
65 nm Process

0.57 um^2 cell
70 Mbit
110 mm^2
April ‘04



45 nm Process

0.346 um^2 cell
153 Mbit
119 mm^2
January ‘06



32 nm Process

0.182 um^2 cell
291 Mbit
118 mm^2
September ‘07

New SRAM test vehicle developed every 2 years to lead development of logic technologies

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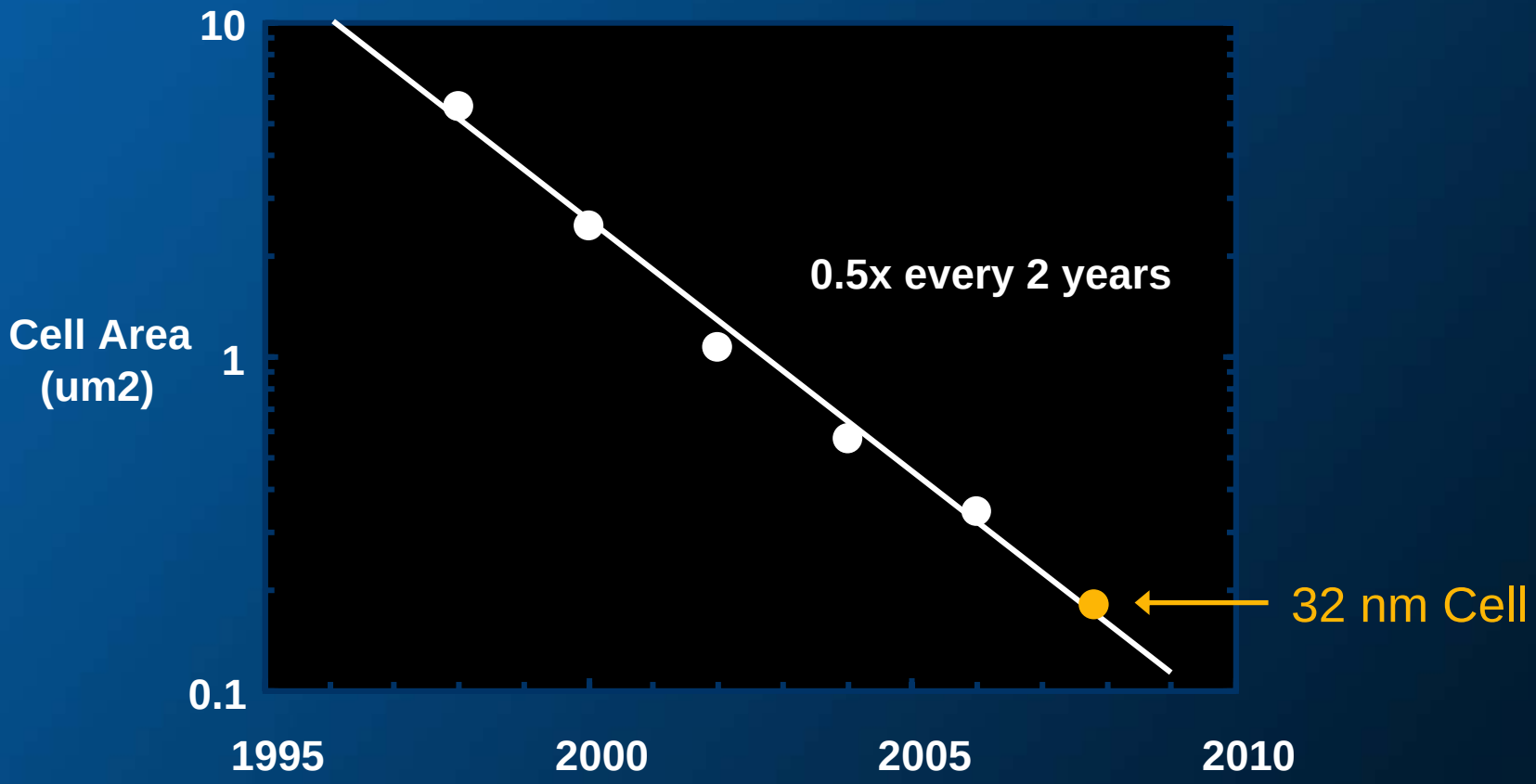
Intel SRAM Cell Size Trend

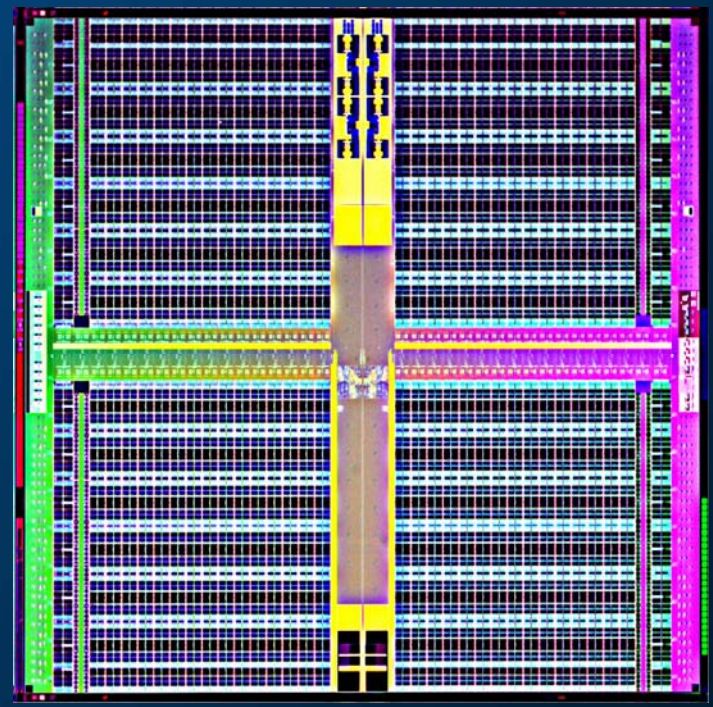


The smaller the SRAM cell, the more transistors that can be packed on a chip and utilized for more features

Transistor density continues to double every 2 years

32 nm SRAM Chip

- 0.182 um^2 cell size
- 291 Mbit, >1.9 billion transistors
- 118 mm^2 chip size
- 2nd gen. high-k + metal gate transistors
- 193 nm immersion lithography on critical layers
- 193 nm dry or 248 nm dry litho on less critical layers
- Functional silicon in Sept '07



32 nm SRAM test vehicle includes all transistor and interconnect features to be used on 32 nm microprocessors

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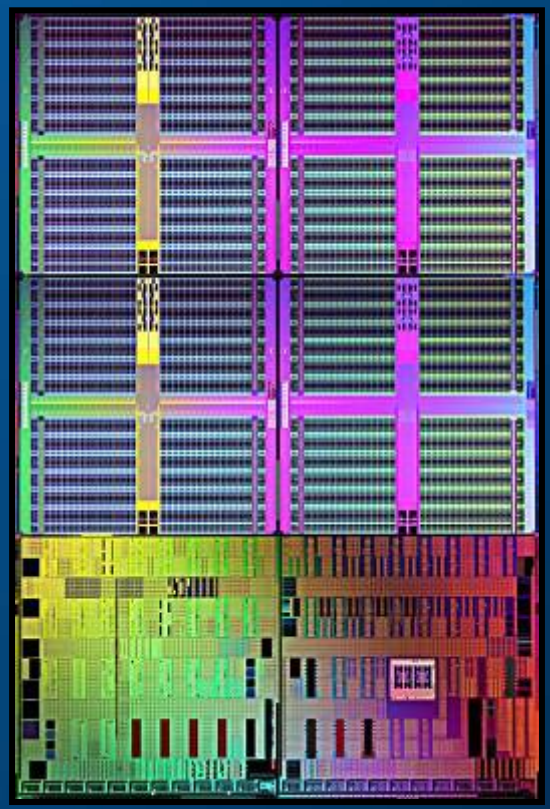
32 nm Test Chip



291 Mbit SRAM

SRAM array
PROM array
High speed register file
High speed I/O circuits
High frequency PLL/Clock

Discrete test structures

32 nm design-for-manufacturability (DFM) test chip includes SRAM and Logic circuits for microprocessors

DFM allows early co-optimization of process and design

Summary

- Intel's 32 nm logic technology has been demonstrated on functional 291 Mbit SRAM chips with >1.9 billion transistors
- These SRAM test chips exercise all transistor and interconnect features to be used on 32 nm microprocessors, including 2nd generation high-k + metal gate transistors
- 32 nm technology will provide significant density, performance and power improvements over today's 45 nm technology
- No other company has demonstrated this level of progress on its 32 nm process
- Intel is on track for 32 nm ramp in 2009